AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1. (Currently Amended) An information processing apparatus comprising:

receiving means having a plurality of inputs for respectively receiving a request signal for requesting bus acquisition for each of a plurality of modules including an encoder and a decoder;

measurement means for measuring a time limit of each of said plurality of modules based on the request signal received by each of said plurality of inputs of said receiving means;

priority determination means for determining a priority of bus acquisition of said plurality of modules according to the time limit measured by said measurement means; and

control means for controlling acquisition of the bus for said plurality of modules based on the priority determined by said priority determination means~~.~~,

wherein said step of determining priority determines said priority of bus acquisition by a first result of judging whether the request signal is received from said encoder or said decoder and a second result of judging whether the request signal is received from the other of said modules based on said first result.

Claim 2. (Previously Presented) The information processing apparatus according to Claim 1, wherein said priority determination means determines priority by means of a round-robin method when there is a plurality of modules having a same time limit as measured by said measurement means.

Claim 3. (Currently Amended) An information processing method comprising the steps of:

receiving a request signal for requesting bus acquisition

for each of a plurality of modules <u>including an encoder and a decoder</u>;

measuring a time limit of each of said plurality of modules based on a request signal requesting bus acquisition received for each of the plurality of modules;

determining priority of bus acquisition of said plurality of modules according to a time limit as measured in said of measuring; and

controlling acquisition of the bus for said plurality of modules based on the priority as determined in said step of determining priority~~.~~<u>,</u>

<u>wherein said priority determination means determines said priority of bus acquisition by a first result of judging whether the request signal is received from said encoder or said decoder and a second result of judging whether the</u>

request signal is received from the other of said modules based on said first result.

Claim 4. (Canceled)

Claim 5. (Canceled)